Notice of Allowability	Application No.	Applicant(s)	
	10/802,895	MILLS ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 1/4/05*.

2. ☒ The allowed claim(s) is/are *1and 3-27*.

3. ☒ The drawings filed on *16 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 1-27 are allowed.

2. The following is an examiner's statement of reasons for allowance: a binary serialization system in which numbers are each encoded as one or more four-bit nibbles, three bits of a nibble are for encoding some portion of a number and one bit of the nibble is for indicating whether encoding of the number is continued to another nibble, a begin command and an end command are used to bracket and thereby group selected nibbles is claimed. The numbers and the commands are serialized in a stream. An interpreter of the stream reads the numbers into data fields of a data object starting at the begin command. The interpreter automatically skips to the end command when the data fields are filled. This type of binary serializer has not been shown in the prior art.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al disclose A method for coding a line code used for a transmission, an interconnection and storing apparatus, comprising:
a first step for adding a one redundancy bit with respect to a n-bit (n represents an odd number higher than 3) source data to generate a pre-code; a second step for setting the pre-code as a code word when a disparity of the pre-code generated in the first step is 0 and the source data is not an in-band signal (or special character);

a third step for inverting a half block (nibble) including a redundancy bit among the bits (block) forming a pre-code when the disparity of the pre-code generated in the first step is 0 and the source data is a set in-band signal (or special character), setting the nibble-inverted pre-code as a code word and generating a complement code word which is a block-inverted code word version and a code word; a fourth step for nibble-inverting a pre-code when the disparity of the pre-code generated in the first step is not 0, setting a nibble-inverted pre-code as a code word when the disparity of the nibble-inverted pre-code is within a predefined value and generating a complement code word which is a block-inverted code word and a code word when the disparity of the set code word is not 0; a fifth step for nibble-inverting the pre-code when the disparity of the pre-code generated in the first step is not 0, manipulating the bits of the pre-code when the disparity of the nibble-inverted pre-code is not within a predefined value, manipulating the bits of the pre-code so that the disparity of the nibble-inverted pre-code is within a predefined value when the disparity of the manipulated pre-code is 0 and concurrently manipulated, setting the manipulated and nibble-inverted pre-code as a code word, and generating a complement code word which is a block-inverted code word version and a code word when the disparity of the set code word is not 0; a sixth step for selecting a code word in which the absolute value of the running digital sum (RDS) is decreased when the code with respect to the source data exists as two values of a complement code word and a code word; and a seventh step for combining the code words for a frame synchronization and generating a synchronization code word so that a pattern is

formed from a serial bit stream when the code word is converted from a parallel form to a serial form.

Obara discloses A random access memory device with a read-out mode operation and a write-in mode operation, said write-in mode operation having a random access stage followed by a simultaneous access stage, comprising: (a) plural memory cell arrays each having a plurality of memory cells arranged in rows and columns; (b) addressing means operative to produce a bit control signal and internal address signals specifying certain memory cells each selected from each memory cell array for said read-out mode operation and said write-in mode operation, one of said certain memory cells being directly specified by a row address signal and a column address signal supplied from an external source; (c) plural read/write switching circuits associated with said plural memory cell arrays, respectively, each of said read/write switching circuits being provided with a write-in switch and a read-out switch which are capable of electrically connecting each of said certain memory cells through said addressing means; (d) plural data amplifier circuits paired with said read/write switching circuits, respectively, each of said data amplifier circuits being provided with a write data amplifier and a read data amplifier which are coupled to said write-in switch and said read-out switch, respectively; (e) a data input buffer circuit supplied with a new data bit from said external source; (f) a data output buffer circuit operative to transfer data bits preserved in said certain memory cells to an external destination in sequence; (g) switching means provided with plural switching transistors having respective conduction paths coupled at one ends thereof to said data amplifier circuits, respectively, and at the other ends

thereof to said data input buffer circuit or said data output buffer circuit; (h) a data control circuit responsive to said bit control signal and operative to cause one of said switching transistors to turn on in said write-in mode operation, said data control circuit being further operative to cause said switching transistors to successively turn on in said read-out mode operation; and (i) a read/write control circuit operative to produce first and second activation signals the former of which is supplied to said write-in switches and said write data amplifiers for activation and the latter of which is supplied to said read-out switches and said read data amplifiers, said first activation signal allowing said write-in switch of one of said read/write switching circuit and said write data amplifier of one of said data amplifier circuits to transfer said new data bit to said memory cell directly specified by said row and column address signals in said random access stage, said second activation signal allowing said read-out switches of said read/write switching circuits except for said one of said read/write switching circuits and said read data amplifiers of said data amplifier circuits except for said one of said data amplifier circuits to read out said data bits from said certain memory cells except for said certain memory cell directly specified by said row and column address signals in said random access stage, said first activation signal allowing all of said write-in switches and all of said write data amplifiers to write said new data bit and said data bits into certain memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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